

WHAT IS CLAIMED IS:

1. A method of fabricating a multi-chip module, comprising:
 - partitioning an integrated circuit design to include a first circuit segment and a second circuit segment, wherein functionality associated the first circuit segment and functionality associated with the second circuit segment jointly enable functionality of the integrated circuit design;
 - fabricating a first semiconductor device capable of enabling said functionality associated with the first circuit segment and including an array of first device interconnect pads;
 - fabricating a second semiconductor device capable of enabling said functionality associated with the second circuit segment and including an array of second device interconnect pads; and
 - facilitating direct interconnection between each one of said first device interconnect pads and a corresponding one of said second device interconnect pads.
2. The method of claim 1 wherein partitioning the integrated circuit design to include a first circuit segment and a second circuit segment includes defining a first functional block of the integrated circuit design and a second functional block of the integrated circuit design.
3. The method of claim 2 wherein defining the first functional block and the second functional block includes defining a memory functional block and a logic functional block, respectively.
4. The method of claim 1 wherein partitioning the integrated circuit design to include a first circuit segment and a second circuit segment includes partitioning the integrated circuit design such that the first circuit segment is associated with a first type of semiconductor substrate and the second circuit segment is associated with a second type of semiconductor substrate.

5. The method of claim 1 wherein partitioning the integrated circuit design to include a first circuit segment and a second circuit segment includes partitioning the integrated circuit design such that the first circuit segment is associated with a first semiconductor fabrication process and the second circuit segment is associated with a second semiconductor fabrication process.

6. The method of claim 1 wherein:
 fabricating the first semiconductor device includes fabricating the first semiconductor device for being capable of enabling functionality associated with a first functional block of the integrated circuit design; and
 fabricating the second semiconductor device includes fabricating the second semiconductor device for being capable of enabling functionality associated with a second functional block of the integrated circuit design.

7. The method of claim 1 wherein:
 fabricating the first semiconductor device includes fabricating a DRAM device; and
 fabricating the second semiconductor device includes fabricating a logic device.

8. The method of claim 1 wherein:
 fabricating the first semiconductor device includes fabricating the first semiconductor device from a first type of semiconductor substrate; and
 fabricating the second semiconductor device includes fabricating the second semiconductor device from a second type of semiconductor substrate.

- 1 9. The method of claim 1 wherein:
2 fabricating the first semiconductor device includes fabricating the first semiconductor
3 device using a first semiconductor fabrication process; and
4 fabricating the second semiconductor device includes fabricating the second
5 semiconductor device using a second semiconductor fabrication process.
- 1 10. The method of claim 1 wherein facilitating direct interconnection between each one of
2 said first device interconnect pads and a corresponding one of said second device
3 interconnect pads includes forming a solder-type interconnect between each one of said
4 first device interconnect pads and the corresponding one of said second device
5 interconnect pads.
- 1 11. The method of claim 10 wherein forming the solder-type interconnect includes forming a
2 solder bump interconnect.
- 1 12. The method of claim 10 wherein forming the solder-type interconnect includes forming a
2 solderball ball interconnect.

- 1 13. A method of fabricating a multi-chip module, comprising:
2 partitioning an integrated circuit design to include a first functional block and a second
3 functional block, wherein functionality associated the first functional block and
4 functionality associated with the second functional block jointly enable
5 functionality of the integrated circuit design;
6 fabricating a first semiconductor device capable of enabling said functionality associated
7 with the first functional block and including an array of first device interconnect
8 pads;
9 fabricating a second semiconductor device capable of enabling said functionality
10 associated with the second functional block and including an array of second
11 device interconnect pads; and
12 facilitating a solder-type interconnect directly between each one of said first device
13 interconnect pads and a corresponding one of said second device interconnect
14 pads.
- 1 14. The method of claim 13 wherein partitioning the integrated circuit design to include the
2 first functional block and the second functional block includes defining a memory
3 functional block and a logic functional block, respectively.
- 1 15. The method of claim 13 wherein partitioning the integrated circuit design to include a
2 first functional block and a second functional block includes partitioning the integrated
3 circuit design such that the first functional block is associated with a first type of
4 semiconductor substrate and the second functional block is associated with a second type
5 of semiconductor substrate.

- 1 16. The method of claim 13 wherein partitioning the integrated circuit design to include a
2 first circuit functional block and a second functional block includes partitioning the
3 integrated circuit design such that the first functional block is associated with a first
4 semiconductor fabrication process and the second functional block is associated with a
5 second semiconductor fabrication process.
- 1 17. The method of claim 13 wherein forming the solder-type interconnect includes forming a
2 solder bump interconnect.
- 1 18. The method of claim 13 wherein forming the solder-type interconnect includes forming a
2 solder ball interconnect.

- 1 19. A multi-chip module, comprising:
2 a first semiconductor device capable of enabling functionality associated with a first
3 circuit segment of an integrated circuit design and including an array of first
4 device interconnect pads;
5 a second semiconductor device capable of enabling functionality associated with a second
6 circuit segment of the integrated circuit design and including an array of second
7 device interconnect pads; and
8 a plurality of device interconnect members, each one of said device interconnect members
9 being electrically connected directly between one of said first device interconnect
10 pads and a corresponding one of said second device interconnect pads.
- 1 20. The multi-chip module of claim 19 wherein:
2 the first semiconductor device includes is capable of enabling functionality associated
3 with a first functional block of the integrated circuit design; and
4 the second semiconductor device is capable of enabling functionality associated with a
5 second functional block of the integrated circuit design.
- 1 21. The multi-chip module of claim 19 wherein:
2 the first semiconductor device is a DRAM device; and
3 the second semiconductor device is a logic device.
- 1 22. The multi-chip module of claim 19 wherein:
2 the first semiconductor device is made from a first type of semiconductor substrate; and
3 the second semiconductor device is made from a second type of semiconductor substrate.
- 1 23. The multi-chip module of claim 19 wherein each one of said device interconnect
2 members is a solder-type interconnect member.

1 24. The multi-chip module of claim 23 wherein the solder-type interconnect member is a
2 solder bump.

1 25. The multi-chip module of claim 23 wherein the solder-type interconnect member is a
2 solder ball.

- 1 26. A multi-chip module, comprising:
2 a first semiconductor device capable of enabling functionality associated with a first
3 functional block of an integrated circuit design and including an array of first
4 device interconnect members;
5 a second semiconductor device capable of enabling functionality associated with a second
6 functional block of the integrated circuit design and including an array of second
7 device interconnect members; and
8 a plurality of solder-type interconnect members, each one of said solder-type interconnect
9 members being electrically connected directly between one of said first device
10 interconnect members and a corresponding one of said second device interconnect
11 members.
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27. The multi-chip module of claim 26 wherein:
28 the first semiconductor device is a DRAM device; and
29 the second semiconductor device is a logic device.
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- 1 31. An electronic package, comprising:
 2 an interposer circuit including a dielectric substrate and an array of routing elements
 3 attached to the dielectric substrate;
 4 a first semiconductor device capable of enabling functionality associated with a first
 5 circuit segment of an integrated circuit design and including an array of first
 6 device interconnect pads;
 7 a second semiconductor device capable of enabling functionality associated with a second
 8 circuit segment of the integrated circuit design, including an array of second
 9 device interconnect pads and including a set of package-level interconnect pads;
 10 a plurality of device interconnect members, each one of said device interconnect members
 11 being electrically connected directly between one of the said first device
 12 interconnect pads and a corresponding one of said second device interconnect
 13 pads; and
 14 a plurality of package-level interconnect members, each one of said package-level
 15 interconnect members being electrically connected between one of the said
 16 package-level interconnect pads of the second semiconductor device and a
 17 corresponding one of said routing elements of the interposer circuit.
- 1 32. The electronic package of claim 31 wherein:
 2 the first semiconductor device includes is capable of enabling functionality associated
 3 with a first functional block of the integrated circuit design; and
 4 the second semiconductor device is capable of enabling functionality associated with a
 5 second functional block of the integrated circuit design.
- 1 33. The electronic package of claim 31 wherein:
 2 the first semiconductor device is a DRAM device; and
 3 the second semiconductor device is a logic device.

- 1 34. The electronic package of claim 31 wherein:
2 the first semiconductor device is made from a first type of semiconductor substrate; and
3 the second semiconductor device is made from a second type of semiconductor substrate.
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- 1 35. The electronic package of claim 31 wherein each one of said device interconnect
2 members is a solder-type interconnect member.
- 1 36. The electronic package of claim 35 wherein the solder-type interconnect member is a
2 solder bump.
- 1 37. The electronic package of claim 35 wherein the solder-type interconnect member is a
2 solderball.
- 1 38. The electronic package of claim 31 wherein:
2 the interposer circuit is a flip-chip interposer circuit; and
3 each one of said package-level interconnect members is a solder-type interconnect
4 member.
- 1 39. The electronic package of claim 31 wherein:
2 the interposer circuit is a wire-bond interposer circuit; and
3 each one of said package-level interconnect members is a conductive wire.

1 40. An electronic package, comprising:
 2 an interposer circuit including a dielectric substrate and an array of routing elements
 3 attached to the dielectric substrate;
 4 a first semiconductor device capable of enabling functionality associated with a first
 5 functional block of an integrated circuit design and including an array of first
 6 device interconnect members;
 7 a second semiconductor device capable of enabling functionality associated with a second
 8 functional block of the integrated circuit design and including an array of second
 9 device interconnect members; and
 10 a plurality of solder-type interconnect members, each one of said solder-type interconnect
 11 members being electrically connected directly between one of the said first device
 12 interconnect members and a corresponding one of said second device interconnect
 13 members; and
 14 a plurality of package-level interconnect members, each one of said package-level
 15 interconnect members being electrically connected between one of the said
 16 package-level interconnect pads of the second semiconductor device and a
 17 corresponding one of said routing elements of the interposer circuit.

1 41. The electronic package of claim 40 wherein:
 2 the first semiconductor device is a DRAM device; and
 3 the second semiconductor device is a logic device.

1 42. The electronic package of claim 40 wherein:
 2 the first semiconductor device is made from a first type of semiconductor substrate; and
 3 the second semiconductor device is made from a second type of semiconductor substrate.

1 43. The electronic package of claim 40 wherein the solder-type interconnect member is a
 2 solder bump.

1 44. The electronic package of claim 40 wherein the solder-type interconnect member is a
2 solder ball.

1 45. The electronic package of claim 40 wherein:
2 the interposer circuit is a flip-chip interposer circuit; and
3 each one of said package-level interconnect members is a solder-type interconnect
4 member.

1 46. The electronic package of claim 40 wherein:
2 the interposer circuit is a wire-bond interposer circuit; and
3 each one of said package-level interconnect members is a conductive wire.